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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MAIS, MARK A	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/779,466	MORRIS, MATT	
	Examiner	Art Unit	
	Mark A. Mais	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 16 February 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 2/16/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statement (IDS) was filed on February 16, 2004. The submission is in compliance with the provisions of 37 C.F.R. 1.97. According, the examiner considered the IDS.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Chapman et al. (USP 6,304,552).

5. With regard to claims 1 and 3, Chapman et al. discloses a stream routing unit **[lossy switch, Abstract]** for routing each of a plurality of input packet streams to any of a plurality of destinations, the stream routing unit comprising:

a plurality of input ports **[input ports, Abstract]** for receiving respective input streams;

a plurality of output ports **[output ports, Abstract]** associated with respective destinations to which the input packet streams can be routed;

storage means for holding packets of the input packet streams at addressable locations each identifiable by an address **[input buffers, col. 2, lines 4-5]**;

an assignment data structure identifying for each input stream at least one destination to which each input packet stream is to be routed **[switch fabric, col. 3, lines 34; col. 6, lines 6-21 (interpreted as a matrix--claim 3)]**; and

a packet allocation data structure holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held, the packet allocation data structure further holding information identifying the intended destination of the packet derived from the assignment data structure **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is inherent in a memory-mapping scheme that the location/address (within the**

buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers].

6. With regard to claim 2, Chapman et al. discloses that the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports **[the input rates are much lower than the output rates, col. 2, lines17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)]**.

7. With regard to claim 4, Chapman et al. discloses that the packet allocation data structure is an array of slots, each slot holding a source identifier and associated address **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57]**.

8. With regard to claim 5, Chapman et al. discloses that the packet allocation data structure is associated with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific**

port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24].

9. With regard to claim 6, Chapman et al. discloses that information identifying the intended destination of the packet is provided by a set of destination pointers, each destination pointer associated with a respective output port and each destination pointer being configured to point to a slot in the array which holds a source identifier and address of a packet intended for a particular destination associated with a particular output port [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24]**.

10. With regard to claim 7, Chapman et al. discloses that the packets of a said input stream are of a common length **[interpreted as common length IP packets, col. 5, lines 62-67]**.

11. With regard to claim 8, Chapman et al. discloses a data communication system **[network, col. 1, lines 36-38]** for routing incoming packets to at least one destination, the system comprising:

a plurality of packet stream sources each generating a packet stream **[multiple input sources for each input port (connects to other users, switches, network elements, col. 5, lines 61-62]**; a stream routing unit **[lossy switch, Abstract]** comprising:

a plurality of input ports **[input ports, Abstract]** for receiving respective input streams;

a plurality of output ports **[output ports, Abstract]** associated with respective destinations to which the input packet streams can be routed;

storage means for holding packets of the input packet streams at addressable locations each identifiable by an address **[input buffers, col. 2, lines 4-5]**;

an assignment data structure identifying for each input stream at least one destination to which each input packet stream is to be routed **[switch fabric, col. 3, lines 34; col. 6, lines 6-21 (interpreted as a matrix--claim 3)]**; and

a packet allocation data structure holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held, the packet allocation data structure further holding information identifying the intended destination of the packet derived from the assignment data structure **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is inherent in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers]**; and

a plurality of destinations for receiving packets of the packet streams generated by the sources **[multiple outputs for each output port (connects to other users, switches, network elements, col. 5, lines 61-62]**.

12. With regard to claim 9, Chapman et al. discloses that at least one of the destinations comprises a programmable transport interface **[interpreted as a repeater, col. 12, lines 15-28]**.

13. With regard to claim 10, Chapman et al. discloses that the input packet streams have a lower bit rate than output streams into which they are merged at the plurality of output ports **[the input rates are much lower than the output rates, col. 2, lines17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)]**.

14. With regard to claim 11, Chapman et al. discloses a method of routing packet streams **[Abstract]** from a plurality of sources to any of a plurality of destinations, the method comprising:

receiving said packet streams **[multiple input sources for each input port (connects to other users, switches, network elements, col. 5, lines 61-62]**;

identifying for each input packet stream at least one destination to which each input packet stream is to be routed using an assignment data structure **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines**

65-67; it holds the source address, col. 10, lines 5-12; it is inherent in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers];

holding each packet of the packet stream at an addressable location identifiable by an address in a storage means address **[input buffers, col. 2, lines 4-5]**;

holding for each new incoming packet a source identifier identifying the origin of the packet and the address in the storage means where the packet is held **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57]**;

holding information identifying the intended destination of the packet derived from the assignment data structure **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57]**; and

using said information identifying the intended destination to route the packet from the storage means to the or each output port **[output ports, Abstract]** associated with the respective identified destination(s) **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers]**.

15. With regard to claim 12, Chapman et al. discloses that the input packet streams have a lower bit rate than output streams into which they are merged at the output ports **[the**

input rates are much lower than the output rates, col. 2, lines17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)].

16. With regard to claim 13, Chapman et al. discloses that the information identifying the intended destination of the packet is provided by a set of destination pointers, said method further comprising:

associating each destination pointer with a respective output port; and configuring each destination pointer to point to a source identifier and address of a packet intended for the destination associated with that output port **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers]**.

17. With regard to claim 14, Chapman et al. discloses holding each new incoming packet in a packet allocation data structure having a plurality of slots;

holding in each slot a source identifier and associated address; and associating each slot with a write pointer which is configured to point to the next available slot in the array for the source identifier and address of the next incoming packet **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is**

using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24].

18. With regard to claim 15, Chapman et al. discloses a device **[lossy switch, Abstract]** for delivering incoming packets to at least one destination **[Abstract]**, the device comprising:

a source to destination matrix for mapping at least one source to at least one destination **[switch fabric, col. 3, lines 34; col. 6, lines 6-21; interpreted as a matrix]**;

a packet allocation table for associating a source and at least one destination for a particular packet with a memory location at which the particular packet is stored **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is inherent in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers]**; and

an algorithm for controlling removal of the incoming packets from a memory to at least one destination **[packet discard, col. 11, lines 58-63]**, wherein the incoming packets have a lower bit-rate than packets delivered to the at least one destination **[the input rates are much lower than the output rates, col. 2, lines17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)]**.

19. With regard to claim 16, Chapman et al. discloses a memory for holding the incoming packets at addressable locations each identifiable by an address **[FIFO buffers, col. 7, line 50 to col. 8, line 10]**; .

20. With regard to claim 17, Chapman et al. discloses a plurality of input ports for receiving respective input packets **[multiple input sources for each input port (connects to other users, switches, network elements, col. 5, lines 61-62]**; and

a plurality of output ports associated with respective destinations to which the input packets can be routed **[multiple outputs for each output port (connects to other users, switches, network elements, col. 5, lines 61-62]**.

21. With regard to claim 18, Chapman et al. discloses a method for delivering incoming packets to at least one destination, the method comprising:

mapping at least one source to at least one destination **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is inherent in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers]]**;

associating a source and at least one destination for a particular packet with a memory location at which the particular packet is stored **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is inherent in a memory-mapping**

scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers]; and

controlling removal of the incoming packets from a memory to at least one destination **[packet discard, col. 11, lines 58-63]**, wherein the incoming packets have a lower bit-rate than packets delivered to the at least one destination **[the input rates are much lower than the output rates, col. 2, lines17-24; especially with bandwidth throttling mechanism, col. 9, lines 2-10; as well as sending HI and LO priority packets (col. 9, lines 28-39)]**.

22. With regard to claim 19, Chapman et al. discloses holding the incoming packets at addressable locations each identifiable by an address **[FIFO buffers, col. 7, line 50 to col. 8, line 10]**.

23. With regard to claim 20, Chapman et al. discloses receiving respective input packets **[multiple input sources for each input port (connects to other users, switches, network elements, col. 5, lines 61-62]**; and

routing outgoing packets through a plurality of output ports associated with respective destinations **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first**

(through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24].

24. With regard to claim 21, Chapman et al. discloses creating a source to destination matrix **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; it is inherent in a memory-mapping scheme that the location/address (within the buffer/queue) of the incoming packet is allocated/used in conjunction with write/read pointers]**.

25. With regard to claim 22, Chapman et al. discloses that he at least one destination is a programmable transport interface **[interpreted as a repeater, col. 12, lines 15-28]**.

26. With regard to claim 23, Chapman et al. discloses that the memory is an SRAM memory **[FIFO buffers, col. 7, line 50 to col. 8, line 10; also RAM memory]**.

27. With regard to claim 24, Chapman et al. discloses a method for controlling removal of packets from a memory to at least one destination **[packet discard, col. 11, lines 58-63]**, the method comprising:

reading each packet from a memory; determining if each packet is destined for more than one destination **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress**

queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24];

if the packet is destined for more than one particular destination, outputting the packet when a port for each particular destination is available [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24**]; and

if the packet is destined for one particular destination, outputting the packet only when a port for the particular destination is free [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24**].

28. With regard to claim 25, Chapman et al. discloses forming an array for indicating, for each packet, a source and destination for a packet held in a particular memory location [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24**].

29. With regard to claim 26, Chapman et al. discloses assigning, for each destination, a pointer directed at a particular slot of the array [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24**].

30. With regard to claim 27, Chapman et al. discloses assigning a write pointer to point to a next available slot in the array [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress**

queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24].

31. With regard to claim 28, Chapman et al. discloses an apparatus **[lossy switch, Abstract]** for controlling removal of packets from a memory to at least one destination **[packet discard, col. 11, lines 58-63]**, the apparatus comprising:

a processor for reading each packet from a memory and determining if each packet is destined for more than one destination **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24]**; and

a plurality of outputs for receiving the packet, wherein if the packet is destined for more than one particular destination, the plurality of outputs receiving the packet when a port for each particular destination is available **[a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory**

pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24].

32. With regard to claim 29, Chapman et al. discloses an array for indicating, for each packet, a source and destination for a packet held in a particular memory location [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24]**.

33. With regard to claim 30, Chapman et al. discloses a pointer, assigned for each destination, directed at a particular slot of the array [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24]**.

34. With regard to claim 31, Chapman et al. discloses a write pointer for pointing to a next available slot in the array [**a routing table for mapping destination address of incoming packets to the output port, col. 7, lines 65-67; it holds the source address, col. 10, lines 5-12; e.g., col. 8, lines 38-57; by mapping incoming packets to egress queues/ports, it is inherent that the memory is using write/read memory pointers; interpreted as the situation where the controller transmits HI priority packets first (through a specific port), then, if possible, transmits LO priority packets (the same port or a different port), col. 10, lines 16-24**].

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

(a) Best et al. (USP 7,218,637), System for switching data using dynamic scheduling.

(b) Goldman et al. (USP 7,212,494), In-band must-serve indication from scheduler to switch fabric,

(c) Gupta et al. (USP 6,272,151), Scalable multimedia network.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Mais whose telephone number is 572-272-3138. The examiner can normally be reached on M-Th 5am-4pm.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wing F. Chan can be reached on 571-272-7493. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

December 11, 2007

1/7/08

WING CHAN
SUPERVISORY PATENT EXAMINER